RESEARCH ARTICLE

LASER & PHOTONICS REVIEWS

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High-Precision Automated Setting of Arbitrary Magnitude and Phase of Mach–Zehnder Interferometers for Scalable Optical Computing

Alessandro di Tria, Gabriele Cavicchioli, Pietro Giannoccaro, Francesco Morichetti, Andrea Melloni, Giorgio Ferrari, Marco Sampietro, and Francesco Zanetto*

Photonic technologies offer promising solutions to the power consumption, bandwidth constraints and latency limits of electronic hardware used in high-performance computing and artificial intelligence. Recently, many studies have proposed and successfully demonstrated photonic accelerators based on integrated meshes of Mach–Zehnder interferometers (MZIs), enabling matrix-vector multiplications directly in the optical domain. While being fast and energy efficient, these photonic architectures still struggle to get the required precision for such applications, because setting the complex coefficients of MZI tunable gates with a high accuracy is still an unsolved problem. This work demonstrates high-precision automated setting and stabilization of MZI-based optical gates with a resolution of 7.01 and 8.04 bits for the output power and phase, respectively. Demonstration is achieved on a multistage silicon photonic circuit comprising a coherent input vector generator, an MZI matrix-vector multiplier, and a coherent receiver for phase measurement. The proposed control strategy can configure the MZIs to any desired working point, without any prior calibration or complex algorithm for the correction of hardware non-idealities, and prevents the propagation of programming errors, thus allowing scalability toward optical processors of large size.

from sound[2] and image[3] processing to biomedical engineering.[4] Typically, these algorithms require intensive execution of matrix-vector or matrix-matrix multiplications (MVM and MMM, respectively), leading to high demands in terms of computational power, energy consumption and training time. Graphics processing units (GPUs), tensor processing units (TPUs), and application-specific integrated circuits (ASICs) appear to be the most appealing computing engines to manage this large amount of data, thanks to their intrinsic parallel processing capabilities.[5] However, the bandwidth limitations (<1 GHz) and energy consumption per operation (>0.4 pJ)[6] of these circuits limit further performance scaling at a reasonable cost, creating a significant bottleneck for the advancement of AI models and applications.

A promising platform for high-performance computing is offered by integrated photonics.[7] While a digital core

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ORIGINAL ARTICLE

Unscrambling light—automatically undoing strong mixing between modes

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Propagation of light beams through scattering or multimode systems may lead to the randomization of the spatial coherence of the light. Although information is not lost, its recovery requires a coherent interferometric reconstruction of the original signals, which have been scrambled into the modes of the scattering system. Here we show that we can automatically unscramble optical beams that have been arbitrarily mixed in a multimode waveguide, undoing the scattering and mixing between the spatial modes through a mesh of silicon photonics tuneable beam splitters. Transparent light detectors integrated in a photonic chip are used to directly monitor the evolution of each mode along the mesh, allowing sequential tuning and adaptive individual feedback control of each beam splitter. The entire mesh self-configures automatically through a progressive tuning algorithm and resets itself after significantly perturbing the mixing, without turning off the beams. We demonstrate information recovery by the simultaneous unscrambling, sorting and tracking of four mixed modes, with residual cross-talk of −20 dB between the beams. Circuit partitioning assisted by transparent detectors enables scalability to meshes with a higher port count and to a higher number of modes without a proportionate increase in the control complexity. The principle of self-configuring and self-resetting in optical systems should be applicable in a wide range of optical applications.
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Monolithic Transimpedance Amplifier for On-Chip Light Monitoring in Pure Silicon Photonics

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***Abstract*— We present a transimpedance amplifier for on-chip optical power monitoring monolithically integrated into a pure Silicon Photonics platform, with no modifications to the fabrication process used by commercial foundries. The designed electronic circuit targets the conversion into voltage signals of the electrical current generated by integrated germanium photodiodes, performed directly on the photonic chip. The amplifier, with a transimpedance gain of 10 kΩ, has been characterized and validated to read light signals up to a frequency of 2 MHz and with an intensity down to about −40 dBm. The circuit is suitable for effectively monitoring the behaviour of photonic devices in a vast range of applications, without penalties in the optical functionality or additional fabrication costs. It thus represents a first demonstration of a more general analog electronics integration into pure Silicon Photonics, paving the way to complex on-chip elaboration and processing towards monolithic electronic control of large-scale optical circuits.**

of monolithic electronic-photonic chips, which are expected to be a key enabler for the next-generation electro-optical systems exploiting the unrivaled bandwidth of optical devices and the versatility of CMOS electronics [2]. The option of integrating photonic devices into standard microelectronic stacks has been successfully pursued in high-speed transceivers for optical communications operating at hundreds of Gbit/s [3], [4], where the proximity of front-end and driver circuits to photonic modulators enables a strong reduction of parasitic effects. In these cases, custom monolithic platforms have been developed, where the integration process of photonics and electronics has been reconsidered and optimized to maximize energy and speed performance.

This option however still struggles to gain popularity in those applications where photonic functionalities prevail

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Determining the optimal communication channels of arbitrary optical systems using integrated photonic processors

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Modes of propagation through an optical system are generally defined as the eigensolutions of the wave equation in the system. When propagation occurs through complicated or highly scattering media, however, modes are better identified as the best orthogonal communication channels to send information between sets of input and output apertures. Here we determine the optimal bidirectional orthogonal communication channels through arbitrary and scattering optical systems using photonic processors. The processors consist of meshes of electrically tuneable Mach–Zehnder interferometers in silicon photonics. The meshes can configure themselves based on simple power maximization or minimization algorithms, without external calculations or calibration or any prior knowledge of the optical system. The identification of the communication mode channels corresponds to a singular value decomposition of the entire optical system, autonomously performed by the photonic processors. We observe crosstalk below −30 dB between the optimized channels even in the presence of distorting masks or partial obstructions. In these cases, although the beams bear little resemblance to conventional mode families, they still show orthogonality. These findings offer potential for applications in multimode optical communication systems, promising efficient channel identification, adaptability to dynamic media and robustness against environmental challenges.

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ARTICLE

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Polarization-transparent silicon photonic add-drop multiplexer with wideband hitless tuneability

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Flexible optical networks require reconfigurable devices with operation on a wavelength range of several tens of nanometers, hitless tuneability (i.e. transparency to other channels during reconfiguration), and polarization independence. All these requirements have not been achieved yet in a single photonic integrated device and this is the reason why the potential of integrated photonics is still largely unexploited in the nodes of optical communication networks. Here we report on a fully-reconfigurable add-drop silicon photonic filter, which can be tuned well beyond the extended C-band (almost 100 nm) in a complete hitless (>35 dB channel isolation) and polarization transparent (1.2 dB polarization dependent loss) way. This achievement is the result of blended strategies applied to the design, calibration, tuning and control of the device. Transmission quality assessment on dual polarization 100 Gbit/s (QPSK) and 200 Gbit/s (16-QAM) signals demonstrates the suitability for dynamic bandwidth allocation in core networks, backhaul networks, intra- and inter-datacenter interconnects.

RESEARCH ARTICLE

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Time-Multiplexed Control of Programmable Silicon Photonic Circuits Enabled by Monolithic CMOS Electronics

Francesco Zanetto, Fabio Toso, Vittorio Grimaldi, Matteo Petrini, Andres Martinez, Maziyar Milanizadeh, Alessandro Perino, Francesco Morichetti, Andrea Melloni, Giorgio Ferrari, and Marco Sampietro*

Programmable photonic circuits require an electronic control layer to configure and stabilize the optical functionality at run-time. Such control action is normally implemented by supervising the status of the circuit with integrated light monitors and by providing feedback signals to integrated actuators. This paper demonstrates that the control action can be effectively performed with electrical signals that are time-multiplexed directly on the photonic chip. To this aim, the necessary electronic functionalities are monolithically integrated in a conventional 220 nm silicon photonics platform with no changes to the standard fabrication process. By exploiting a non-conventional structure to implement metal-oxide–semiconductor field-effect transistors, an electronic controller is co-designed into a programmable photonic circuit to enable a time-multiplexed readout of integrated photodetectors and sequential activation of thermal phase shifters with on-chip electronic memory. The accuracy of the time-multiplexed control, achieved on a time scale of less than 10 ms, is demonstrated by penalty-free routing of 10 Gbit s^{-1} modulated signals. This approach can be straightforwardly applied to large-scale photonic chips to reduce the number of required electrical input/output connections.

to program the overall photonic functionality. A real-time active control layer, currently implemented by electronic feedback loops through external circuitry connected to on-chip light sensors and actuators, is thus needed to ensure reliable optical operations.[2–10] Although effective, the scaling of this approach is limited by the number of required electrical input/output (I/O) connections,[11,12] that approaches a prohibitive level in large-scale architectures. Flip-chip electronic-photonic interconnection via copper-pillar technology[13] enables larger I/O port counts with respect to wire bonding, yet implying extra assembly and packaging costs.

Monolithic integration of electronics and photonics on the same technological platform is envisioned as a way not only to overcome the electrical I/Os bottleneck but also to equip photonic chips with new enabling functionalities.[14–16] Build-

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Unconventional Monolithic Electronics in a Conventional Silicon Photonics Platform

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***Abstract*— To enrich state-of-the-art optical chips with electronic functionalities, we present the integration of unconventional transistors and circuits in a standard silicon photonics platform, with no modifications to the conventional fabrication process employed by photonic foundries. This approach allows us to include on-chip electronic building blocks to support the optical functionality at zero additional cost while maintaining optical excellence and foundry interoperability. To showcase the benefits of monolithic electronics, we integrated a transconductance amplifier and an analog multiplexer for sequential readout of 16 photodetectors, distributed in a large-scale architecture of Mach–Zehnder interferometers (MZIs). The circuits, successfully validated in optical experiments, allow the reduction of electrical input-output lines of a photonic chip without any optical penalty, thus targeting one of the main bottlenecks that limit further scaling of photonic circuits.**

merged to obtain high-performance electro-optical systems. When the electronic functionalities needed in a photonic chip are prevailing, as, for example, in high-speed transceivers for optical communications operating at hundreds of Gbit/s, the option of integrating the photonic devices into a standard microelectronic stack has been successfully pursued [1], [2], [3], [4].

In many other cases, such as optical computers, neuromorphic systems, and quantum photonic processors [5], [6], [7], photonic functionalities prevail and excellent optical performance is required. Given the relatively large size of photonic circuits, specialized photonic foundries simplified the stack of standard microelectronic processes, which is no longer necessary, by selecting only a few essential steps to reduce costs while allowing for low-loss optical devices. The electronic

1/f Noise Characteristics of Waveguide-Integrated PbTe MIR Detectors and Impact on Limit of Detection

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***Abstract*—The noise power spectral density of a detector is essential for determining the frequency of operation and readout architecture that yields an optimal signal-to-noise ratio. In this work, we characterize a waveguide-integrated PbTe mid-infrared detector and report on its noise spectrum, highlighting the presence of a current-dependent 1/f term dominating at low frequency and/or high bias over the Johnson component typical of a photoconductor. This behaviour, together with the substantially flat frequency response in the range between 1 kHz to 1 MHz, guide towards a lock-in readout strategy, that allows one to operate in the region of minimum noise without penalties in the detection performance. Practical guidelines to optimize the readout resolution are provided and the limit of detection of a gas sensing system exploiting PbTe photoconductors is derived, as an example of how a careful co-design of sensors and electronics can dramatically improve the detection performance.**

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Differential Impedance Sensing platform for high selectivity antibody detection down to few counts: A case study on Dengue Virus

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ABSTRACT

We developed a biosensing system for serological detection of viruses based on the impedance variation between gold microelectrodes upon the capture of the target antibodies hybridized with nanobeads for signal amplification. The microfluidic platform core features a Differential Impedance Sensing (DIS) architecture between a reference and an active sensor able to reach nanoparticle resolution of few tens. The biosensor, functionalized with a copoly layer housing a synthetic peptide probe, has shown a limit of detection (LOD) below 100 pg/mL using a model IgG antibody spiked in a buffer. The biosensor was also tested with human serum samples for quantitative counts of anti-Dengue Virus antibodies, reaching a sensitivity that outperforms commercial ELISA kit. The system is perfectly suited to be easily reconfigured for novel probes by simply modifying the preparation of the biosensor chip surface, thus addressing a wide range of pathogens and diseases with clinically relevant concentrations for rapid immunoassays in a point of care setting.

Optics Letters

High-sensitivity transparent photoconductors in voltage-controlled silicon waveguides

ALESSANDRO PERINO,[1,*] FRANCESCO ZANETTO, MATTEO PETRINI, FABIO TOSO, FRANCESCO MORICHETTI, ANDREA MELLONI, GIORGIO FERRARI, AND MARCO SAMPIETRO

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On-chip optical power monitors are essential elements to calibrate, stabilize, and reconfigure photonic integrated circuits. Many applications require in-line waveguide detectors, where a trade-off has to be found between large sensitivity and high transparency to the guided light. In this work, we demonstrate a transparent photoconductor integrated on standard low-doped silicon-on-insulator waveguides that reaches a photoconductive gain of more than 10^6 and an in-line sensitivity as high as −60 dBm. This performance is achieved by compensating the effect of electric charges in the cladding oxide through a bias voltage applied to the chip substrate or locally through a gate electrode on top of the waveguide, allowing one to tune on demand the conductivity of the core to the optimum level.

free-carrier generation occurring in the WG core due to surface state absorption to realize integrated PDs [4] and photoresistors [5–7]. The main drawback of subbandgap detectors is the small signal they provide, which increases the complexity of the readout electronics. This aspect can be solved by exploiting the intrinsic gain mechanism of photoresistors [8]. Transparent photoresistors have been demonstrated in the literature but they have often been proposed with an additional doping of the WG core of about 10^{17} cm^{-3}, a level that increases the WG attenuation.

We propose an integrated photoresistor directly made on the low-doped silicon layer of a standard Silicon Photonics SOI technology, which overcomes these limitations and demonstrates extremely high sensitivity to light. In contrast to doped devices,

High-Value Tunable Pseudo-Resistors Design

Emanuele Guglielmi, Fabio Toso, Francesco Zanetto, Giuseppe Sciortino, Alireza Mesri, Marco Sampietro, *Member, IEEE*, and Giorgio Ferrari, *Member, IEEE*

***Abstract*— Pseudo-resistor circuits are used to mimic large value resistors and base their success on the reduction of occupied areas with respect to physical devices of equal value. This article presents an optimized architecture of pseudo-resistor, made in standard CMOS 0.35 μm technology to bias a low-noise transimpedance amplifier for high-sensitivity applications in the frequency range 100 kHz–10 MHz. The architecture was selected after a critical review of the different topologies to implement high-value resistances with MOSFET transistors, considering their performance in terms of linearity of response, symmetric dynamic range, frequency behavior, and simplicity of realization. The resulting circuit consumes an area of 0.017 mm^2 and features a tunable resistance from 20 MΩ to 20 GΩ, dynamic offset reduction due to a more than linear I–V curve, and a high-frequency noise well below the one of a physical resistor of equal value. This latter aspect highlights the larger perspective of pseudo-resistors as building blocks in very low-noise applications in addition to the advantage in occupied areas they provide.**

of view, as resistors. They have demonstrated their effectiveness in specific circuits, such as transimpedance amplifiers for high-sensitivity current measurements on nanodevices down to fA [1]–[4], filters showing very large time constants despite the use of small capacitors in the tens of fF range [5], [6], or ultralow noise CMOS current amplifiers [7], [8].

In this article, we target capacitive-feedback architectures that require a resistive feedback path to bias the amplifier and to handle the dc leakage currents that could be present at its input. Capacitive-feedback architectures are indeed a very good option when a pA sensitivity in the current measurement is desired together with high linearity response over a rail-to-rail output voltage and large operating frequency range between 100 kHz and 10 MHz, as it is the case, for example, in the impedance sensing or impedance spectroscopy circuits.

WDM-Based Silicon Photonic Multi-Socket Interconnect Architecture With Automated Wavelength and Thermal Drift Compensation

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***Abstract*—A silicon photonic circuit comprising all the building blocks necessary to demonstrate optical communication between two sockets interconnected through an Arrayed Waveguide Grating Router (AWGR) is reported. The article focuses on the robustness of the interconnection scheme to the unavoidable wavelength and thermal fluctuations observed in real datacenter environments. To improve the reliability of the system, a feedback control mechanism, based on contactless integrated photonic probes (CLIPP) and heater actuators, is added to the interconnection to monitor in parallel the working point of each sensitive device and keep it locked in real-time. Experimental results demonstrate successful operations in a 30 Gbit/s data routing scenario at $5 \cdot 10^{-11}$ bit error rate, irrespective of sudden wavelength shifts of up to 200 pm or of iterated thermal variations in a 10 °C temperature range, with a recovery time of around 30 ms. These results prove that AWGR-based interconnections equipped with real-time drift compensation systems can be a viable option in multi-socket layouts even in highly demanding environments.**

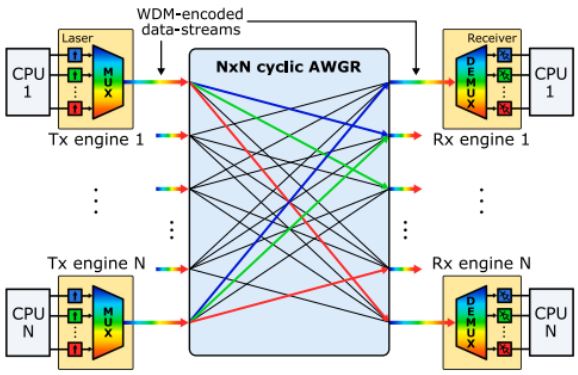

Fig. 1. CPU interconnection scheme proposed within the H2020 ICT-STREAMS European project. Thanks to WDM data encoding and to the